IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

C. Amendments to the Claims.

1. (Original) A memory circuit, comprising:

a plurality of sense amplifier circuits having a predetermined pitch in a first direction; and

a plurality of programmable element controlled devices, each programmable element controlled device fitting within the pitch and isolating at least one associated bitline from a corresponding sense amplifier circuit when disabled.

2. (Original) The memory circuit of claim 1, wherein:

the programmable element controlled devices comprise n-channel insulated gate field effect (IGFET) transistors laid-out within the pitch of the corresponding sense amplifier.

3. (Original) The memory circuit of claim 2, wherein:

each of programmable element controlled devices includes

a first n-channel IGFET having a source-drain path coupled between a first bitline of a bitline pair and the corresponding sense amplifier circuit, and

a second n-channel IGFET having a source-drain path coupled between a second bitline of the bitline pair and the corresponding sense amplifier circuit.

4. (Original) The memory circuit of claim 1, wherein:

each bitline is coupled to a plurality of memory cells selected from the group consisting of one transistor dynamic random access memory (DRAM) type cells, magnetoresistive RAM (MRAM) cells, thyristor RAM (TRAM) cells, and ferromagnetic RAM (FRAM) cells.

5. (Original) The memory circuit of claim 1, wherein:

the bitlines comprise folded bitline pairs, each bitline of a bitline pair being arranged parallel and adjacent to one another.

6. (Original) The memory circuit of claim 1, wherein:

the bitlines comprise open bitline pairs, with one bitline of each pair extending over one array section and the other bitline of each pair extending over a different array section.

7. (Original) The memory circuit of claim 1, wherein:

the bitlines comprise unpaired bitlines, each coupled to a sense amplifier circuit that also receives a reference value to compare with a data signal provided by each bitline.

8. (Original) The memory circuit of claim 1, wherein:

the bitlines are arranged into logical groups each including a plurality of bitline pairs; and

the programmable element controlled devices associated with each logical group are commonly disabled in response to the same control signal.

9. (Currently Amended) A method of reducing a standby current contribution in conductive lines of a memory device, comprising the steps of:

providing at least one transistor between each of a plurality of conductive lines arranged in a first direction within a memory cell array and a corresponding circuit coupled to ~~the~~**a** conductive line, including providing at least one transistor between a bitline and a corresponding sense amplifier circuit;

programming a fuse-type element to generate **and maintain a** control signal first value if an associated conductive line is determined to have a defect; and

disabling each transistor when the associated control signal has the first value to prevent defect induced current from flowing through the transistor with respect to the corresponding conductive line.

10. (Original) The method of claim 9, wherein:

the step of programming the fuse-type element is performed in a wafer test procedure.

Claim 11 (Cancelled)

12. (Previously Presented) The method of claim 9, wherein:

the step of providing at least one transistor includes providing at least one transistor between a bitline and an equalization circuit within the sense amplifier circuit.

13. (Original) The method of claim 9, further including:

the step of providing at least one transistor includes providing at least one transistor between a wordline and a corresponding wordline driver circuit.

14. (Original) A circuit for reducing defect induced standby current in a memory device, comprising:

a plurality of first conductive lines parallel to one another, each first conductive line coupled to a plurality of memory cells in a memory cell array;

a plurality of first circuits arranged on at least one side of the memory array, each first circuit being associated with at least one associated first conductive line and having a same first pitch in a first direction; and

a plurality of first isolation circuits, each first isolation circuit permanently isolating a corresponding first circuit from the associated at

least one first conductive line when activated and fitting within the first pitch.

15. (Original) The circuit of claim 14, wherein:

the plurality of first conductive lines comprise bitlines commonly coupled to memory cells of the same column in the memory cell array; and

the plurality of first circuits comprise sense amplifier circuits for driving an associated bitline according to a data value on such bitline.

16. (Original) The circuit of claim 15, further including:

a plurality of wordlines parallel to one another, each wordline coupled to memory cells of the same row;

a plurality of wordline driver circuits arranged on at least a second side of the memory array, each wordline driver circuit coupled to at least one of the wordlines and having the same pitch in a second; and

a plurality of second isolation circuits, each second isolation circuit permanently isolating a corresponding wordline driver circuit from the associated wordline when activated.

17. (Original) The circuit of claim 14, wherein:

the plurality of first conductive lines comprise wordlines commonly coupled to memory cells of the same row in the memory cell array; and

the plurality of first circuits comprises wordline driver circuits for driving an associated wordline according to an applied address value.

18. (Original) The circuit of claim 14, further including:

at least one fuse circuit for providing an activation signal according to the state of at least one fuse-type element; and

each isolation circuit comprises at least one transistor having a gate coupled to the activation signal.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

19. (Original) The circuit of claim 18, wherein:

the isolation circuit includes a plurality of transistors having gates commonly coupled to the activation signal.

20. (Original) The circuit of claim 18, wherein:

the fuse-type element is selected from the group consisting of: a fusible link alterable to have a conducting or a non-conducting state, an anti-fuse structure alterable to have a conducting or a non-conducting state, an electrically programmable memory cell programmable to have a conducting or a non-conducting state.